Remarks

Applicants thank the Examiner for the careful examination of this application and the clear explanation of the rejections.

The amended title indicates the invention to which the claims are directed.

The amended abstract is in proper form.

The amended specification refers to the issued patent in the parent application

The new claims "particularly point out and distinctly claim the subject matter the applicant regards as his invention."

New independent claim 15 defines a process for testing a circuit having both a vendor embedded circuit core and appended user circuitry, using ATPG software to generate test vectors therefore.

The process generates a partial netlist of the entire vendor circuit.

The process defines at least one pseudo-pin input for at least some of the circuitry in the partial netlist.

The process identifies an output node of the vendor circuit to which the user circuitry will be connected.

The process generates an abbreviated core netlist of the vendor circuit that includes the pseudo-pin input and the output node to produce outputs at the output node in response to an input.

Claim 15 finds support in the disclosure of Figure 3 and accompanying explanatory text.

In contrast, US 5,903,578 to De discloses:

Stated generally, the present invention involves the steps of identifying a first logic group comprising gates within a digital logic block that may be tested using a test port, identifying a second logic group comprising gates that may be tested in isolation from the first logic group, and generating a reduced netlist, the reduced netlist containing netlist information for the second logic group, the netlist containing less than complete netlist information for the first logic group.

In a second aspect of the present invention, a method is provided for connecting scan cells within a logic block removed from the netlist, to the scan chain within the rest of the ASIC. This method avoids revealing to the test pattern generator the existence of those scan cells. According to the method, a first scan chain includes all of the scan cells within the ASIC, including those scan cells that are within the removed logic block. A second chain includes only those scan cells that are not within the removed logic. A command bit selects either the first or the second chain to be connected to the scan output. When the second chain is selected and the data contained within the scan chain read out, knowledge of the existence of scan cells within the removed logic block is not required to determine the expected scan chain output. Because knowledge of the scan cells within the removed logic block is not required, additional information about the removed logic block is kept confidential.

When the first chain is selected, the information within the removed logic block will also be read out, and knowledge of all scan cells within the ASIC will accordingly be required. However, the portion of the test pattern program that exercises the removed logic and reads the information out of the scan cells within the first chain is the portion that is supplied by the ASIC vendor. Therefore, no information about the scan cells within the removed logic block needs to be supplied to the customer or the test pattern generation program being used by the customer. (Paragraph bridging columns 3 & 4 and following)

The De patent fails to teach or disclose the claimed steps of defining at least one pseudo-pin input for at least some of the circuitry in the partial netlist,

identifying an output node of the vendor circuit to which the user circuitry will be connected, and generating an abbreviated core netlist of the vendor circuit that includes the pseudo-pin input and the output node to produce outputs at the output node in response to an input.

US 6,223,315 to Whetsel discloses an intellectual property core and an external register present lead carrying a signal indicating the presence of a scan register.

The Whetsel patent fails to teach or disclose the claimed steps of defining at least one pseudo-pin input for at least some of the circuitry in the partial netlist, identifying an output node of the vendor circuit to which the user circuitry will be connected, and generating an abbreviated core netlist of the vendor circuit that includes the pseudo-pin input and the output node to produce outputs at the output node in response to an input.

The application is in allowable form and the claims distinguish over the cited references. Applicants respectfully request reconsideration or further examination of this application.

Respectfully Submitted,

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